In addition, contact holes (not shown) are opened reaching the N^+ diffusion layer 9a that is a source by several bits at the same time when the contact hole 20 is formed, and the contact holes are embedded by the wiring layer 21. A stay of the wiring layer 22 is provided, and further, an interlayer insulation film is fully formed. Then, a contact hole 23 is formed so as to reach the stay of the wiring layer 22 formed in a source region prior to this interlayer insulation film, is embedded by a wiring layer (not shown), and is commonly connected in a wiring layer, thereby making it possible to make a resistance of a common source line lower than that in a case of only an N^+ diffusion layer.

A1

IN THE DRAWINGS

Please find enclosed copies of Figs. 4 and 5, as originally filed, with proposed amendments indicated in red for the approval of the Examiner. approved 4/23/03 DLD

IN THE CLAIMS

Please cancel claims 3 and 4, without prejudice or disclaimer.

Please rewrite claims 1, 2, 5, and 6, as follows:

Amend B1

1. (Once Amended) A non-volatile semiconductor storage apparatus comprising:

a memory cell array which has unit cells arranged in a rectangular matrix shape, said unit cell including:

A2

a memory cell field effect transistor having a floating gate and a control gate, an insulating layer below said floating gate being used as a tunneling gate oxide layer; and

a select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said floating gate and control gate extending to a position above a

gate of said select field effect transistor, top and bottom surfaces of said floating gate and said control gate in said position being parallel to top and bottom surfaces of said gate of said select field effect transistor.

2. (Once Amended) A non-volatile semiconductor storage apparatus having a memory cell array having unit cells, said unit cell including a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate and a control gate, an insulating layer below said floating gate being used as a tunneling gate oxide layer, and said select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said storage apparatus comprising:

a first semiconductor layer composing a portion of said floating gate and a gate of said select field effect transistor;

a second semiconductor layer formed on said first semiconductor layer in said memory cell field effect transistor, said second semiconductor layer not contacting said tunneling gate oxide layer, a lower surface of said second semiconductor layer being located at a height at least equal to a height of an upper surface of said first semiconductor layer, said second semiconductor layer composing another portion of said floating gate and extending to a position above said gate of said select field effect transistor;

a first insulation layer which insulates said first semiconductor layer from said second semiconductor layer in said select field effect transistor, said first insulation layer contacting said first semiconductor layer;

a second insulation layer formed on said second semiconductor layer; and